

Notice of References Cited	Application/Control No. 09/893,718	Applicant(s)/Patent Under Reexamination NALAWADI ET AL.	
	Examiner James K. Trujillo	Art Unit 2116	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,158,000 A	12-2000	Collins, David L.	713/1
	B	US-6,314,511 B2	11-2001	Levy et al.	712/217
	C	US-6,115,813 A	09-2000	Hobson et al.	713/1
	D	US-6,493,741 B1	12-2002	Emer et al.	718/107
	E	US-6,038,632 A	03-2000	Yamazaki et al.	710/260
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Intel Press Release, "Intel Introduces Fast Processor and Innovative Chipset for Value PCs", [online] April 26, 1999 [retrieved on 2004-09-01]. Retrieved from the Internet:< URL: http://www.intel.com/pressroom/archive/releases/dp042699.htm >.
	V	Intel Dev. Datasheet, "Intel® 810 Chipset: Datasheet", [online] 4-7-04 [retrieved. on 09-01-04]. Internet:< URL: http://web.archive.org/web/20000407104348/http://www.intel.com/design/chipsets/datashts/290656.htm >[using Wayback Machine].
	W	S. J. Eggers et al., "Simultaneous Multithreading: A Platform for the Next-Generation Processors", IEEE Micro, September/October 1997, pages 12-18.
	X	J. Lo et al. "Converting Thread-Level Parallelism Into Instruction-Level Parallelism via Simultaneous Multithreading", ACM Transactions on Computer Systems, August 1997, pages 322-354.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.